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APPLICATION NUMBER: ***60/526,926***
FILING DATE: ***December 03, 2003***
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. EL 753209421 US

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Samuel	Anderson	Tempe, AZ

Additional inventors are being named on the ______ *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

BOND WIRELESS PACKAGE

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☑ Customer Number: 24964

OR

☐ Firm or Individual Name					
Address					
Address					
City		State		Zip	
Country	-	Telephone		Fax	

15535 U.S. PTO
60/526926
120303

ENCLOSED APPLICATION PARTS ***(check all that apply)***

☑ Specification *Number of Pages* 4

☑ Drawing(s) *Number of Sheets* 9

☐ Application Date Sheet. See 37 CFR 1.76

☐ CD(s), Number ______

☐ Other (specify) ______

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☑ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees.

☑ The Director is herby authorized to charge filing fees or credit any overpayment to Deposit Account Number: 06-0923

☐ Payment by credit card. Form PTO-2038 is attached.

FILING FEE Amount ($): $80.00

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☑ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: ______

Respectfully submitted,

SIGNATURE William C. Hwang

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Date December 2, 2003

REGISTRATION NO. 36,169
(if appropriate)
Docket Number: 104023-664-PRO

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

LIBNY/4264971.1

C untry: US
Application No.: TBA
Filing Date: December 2, 2003
Inventor: Samuel Anderson
Title: BOND WIRELESS PACKAGE
Atty Docket No.: 104023-664-PRO

CERTIFICATE OF "EXPRESS MAILING"

"EXPRESS MAIL" Mailing Label Number: EL 753209421 US

Deposited: December 2, 2003

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Submitted herewith are the following items:

1. Provisional Patent Application Transmittal in duplicate (2 pages);
2. U.S. Provisional Patent Application of Samuel Anderson (13 pages);
3. This Certificate of Express Mailing bearing Express Mailing Label No. and deposit date stated above (1 page); and
4. Return Receipt Postcard.

TOTAL PAGES IN THIS SUBMISSION: 16 + postcard

Francene Sawyer

Francene Sawyer

Attorney D cket N .: 104023-664-PRO

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Francene Sawyer December 2, 2003

Francene Sawyer Date

U.S. Provisional Patent Application Entitled

BOND WIRELESS PACKAGE

Inventor(s):

Samuel Anderson of Tempe, AZ

TITLE

[0001] Bond Wireless Package

FIELD OF THE INVENTION

[0002] This invention generally relates to a novel semiconductor package.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] The figures below depict various aspects and features of the present invention in accordance with the teachings herein.

DESCRIPTION OF THE INVENTION

[0004] The aspects, features and advantages of the present invention will become better understood with regard to the following description with reference to the accompanying drawings. What follows are preferred embodiments of the present invention. It should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this description may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined herein and equivalents thereto. Use of absolute terms, such as "will not," "will," "shall," "shall not," "must," and "must not," are not meant to limit the present invention as the embodiments disclosed herein are merely exemplary.

[0005] Figure 1 shows that vertical trench MOSFETs currently dominate the low-voltage discrete market. Low R_{DSON}, ruggedness and low cost contribute to their dominance in these applications. However, high gate charge Q_g is a disadvantage and

RDSON contributed from wafer substrate and wire bond become problematic for MOSFETs with a breakdown voltage rating below 15V. Lateral power MOSFETs, used primarily in power integrated circuits, have low Q_g and improvements in R_{DSON} make them attractive for high frequency power management applications.

[0006] Figure 2 shows a bi-directional switch utilizing lateral power MOSFETs. The novel switch is an interleaved common-drain LDMOS structure. As depicted, the structure uses bump and/or pillar technology for interconnections to a device package such as that shown in Figure 3. A more detailed description of this technology is described in United States Patent Application No. 10/601,121, and United States Provisional Patent Application Nos. 60/444,932 and 60/501,192.

[0007] Figure 4a shows a package according to one aspect of the present invention from a dimensional perspective in contrast to a conventional wire bond package shown in Figure 4b.

[0008] Figure 5a shows a cutaway view of the novel package with an substrate utilizing solder bump (as shown in Figure 2) and/or pillar technology. In particular, Figure 5b shows a substrate with copper-pillar bump interconnect structure. Each bump/pillar preferably connects to one or more sources, drains or gates. Rather than using wire bond, Figure 5c shows depicts a lead structure that connects the bumps to external leads outside the package, preferably using copper.

[0009] Figure 6a shows a package practicing one aspect of the present invention and showing the dimensions of the copper leadframe, solder bump and copper pillar dimensions and die size in contrast with a conventional wire bond package shown in Figure 6b. Figure 7a shows the thermal characteristics of the novel package in contrast to

a conventional wire bond package shown in Figure 7b. Figure 8 is a summary of thermal, electrical and stress characteristics between on embodiment of the novel package and a conventional package using finite element analysis, further discussed in Figure 9.

CONCLUSION

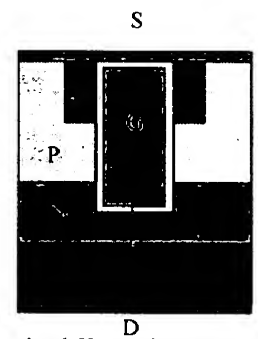
[0010] Having now described preferred embodiments of the invention, it should be apparent to those skilled in the art that the foregoing is illustrative only and not limiting, having been presented by way of example only. All the features disclosed in this specification (including any accompanying claims, abstract, and drawings) may be replaced by alternative features serving the same purpose, and equivalents or similar purpose, unless expressly stated otherwise. Therefore, numerous other embodiments of the modifications thereof are contemplated as falling within the scope of the present invention as defined by the appended claims and equivalents thereto.

[0011] For instance, the exemplary figures show an 8 lead package as one embodiment of the present invention compared to a comparable 8 lead package utilizing conventional wire bond technology. As will be apparent to one skilled in the art, the present invention can be extended to packages with more or less than 8 leads. Likewise, although, for instance, Figures 5 and 6 depict a copper pillar solder bump, other variations such as only a solder bump or pillar made of materials other than copper may be used and the selection of materials to be used as well as the size of these pillars and bumps would be apparent to one skilled in the art depending on factors such as conductivity, parasitic resistance, heat conduction and so on.

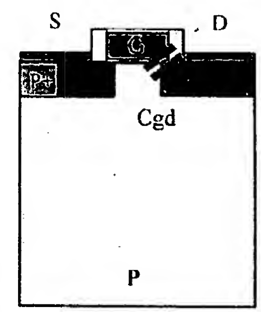
FIGURE 1

MOSFET Structures: Vertical vs. Lateral

- Currently vertical trench MOSFETs dominate the low-voltage discrete market. These devices offer low R_{DSON}, good device ruggedness, and low cost, but suffer from high gate charge Q_g. Furthermore, the R_{DSON} contributions from wafer substrate and wire bond become dominant for MOSFETs with a breakdown voltage rating below 15V.
- Traditionally lateral power MOSFETs are exclusively used in power ICs with a limited die size and current rating. However, their inherently low Q_g and much improved R_{DSON} over the past few years make them very attractive for the high frequency power management applications.



Vertical Trench MOSFET



Lateral MOSFET

C_{gd} (Trench) >> C_{gd} (Lateral) and Q_g (Trench) >> Q_g (Lateral)

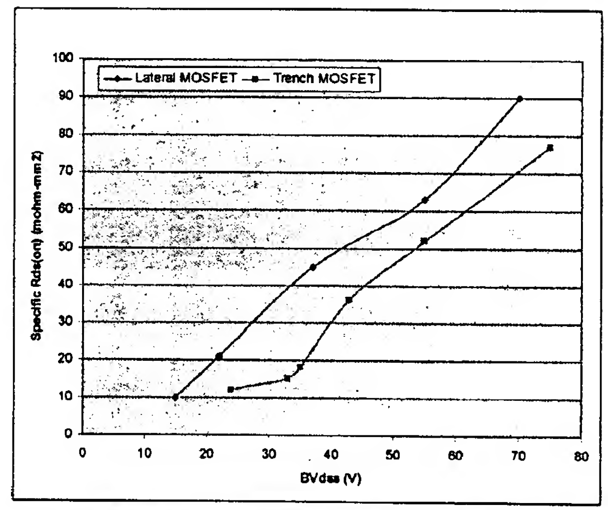
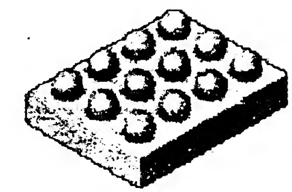


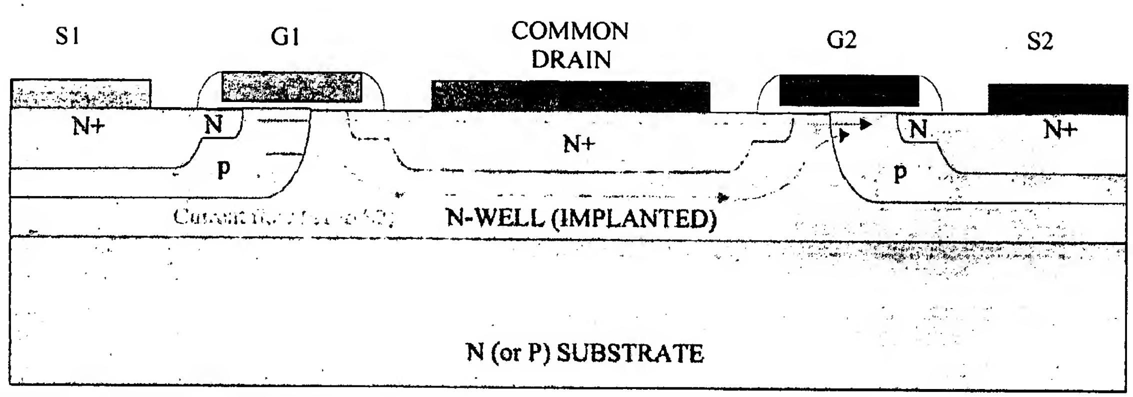
FIGURE 2

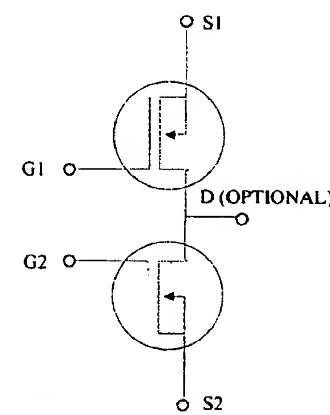
GWS8314: A Bi-Directional Switch

- Novel interleaved common-drain LDMOS structure
- Breakdown voltage BVDSS of greater than 20 V
- Low RDSON of 20 mΩ at VGS of 4.5V
- Small die/package foot print of 2.1 mm by 2.1 mm
  (50% of the die size of the closest trench MOS competition)
- Ultra-low FFOM of 85 mΩ*mm2
- Ultra-low package profile of less than 0.8 μm



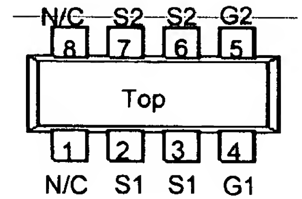
2.1 x 1.6 mm2

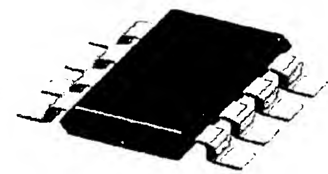


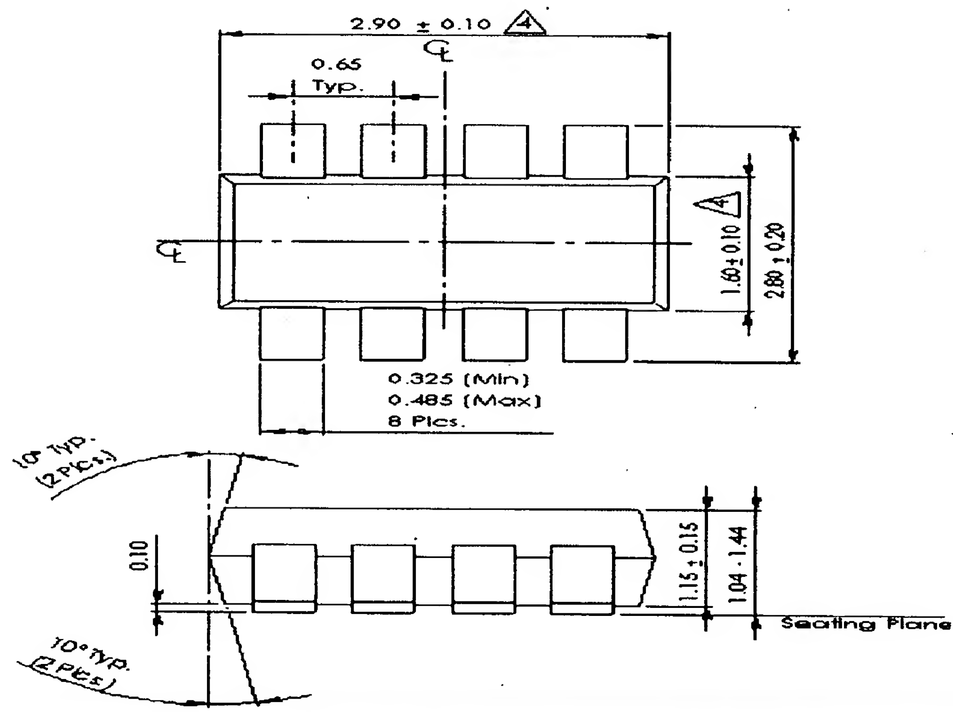


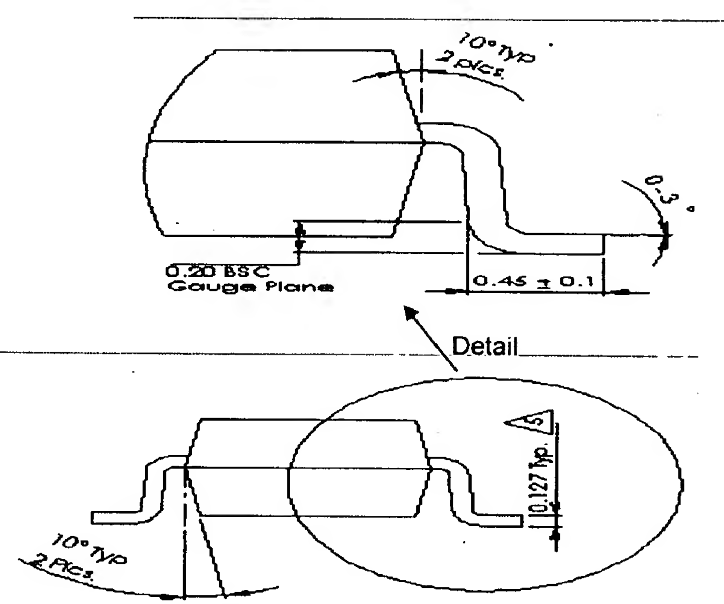
Package Outline Drawing And Pinout: SOT23-8L BW™

Notes:
1. Dimensions and Tolerances per ANSI Y14.5M, 1982.
2. Mirror finish on package surface.
3. Footlength measured based on the gauge plane method.
4. Dimension exclusive of mold flash and gate burr.
5. Dimension exclusive of solder plating.









Model Views and Primary dimensions.

FIGURE 4

Refer to Product Specs for detailed dimensions and information.

GWS6968BW Package

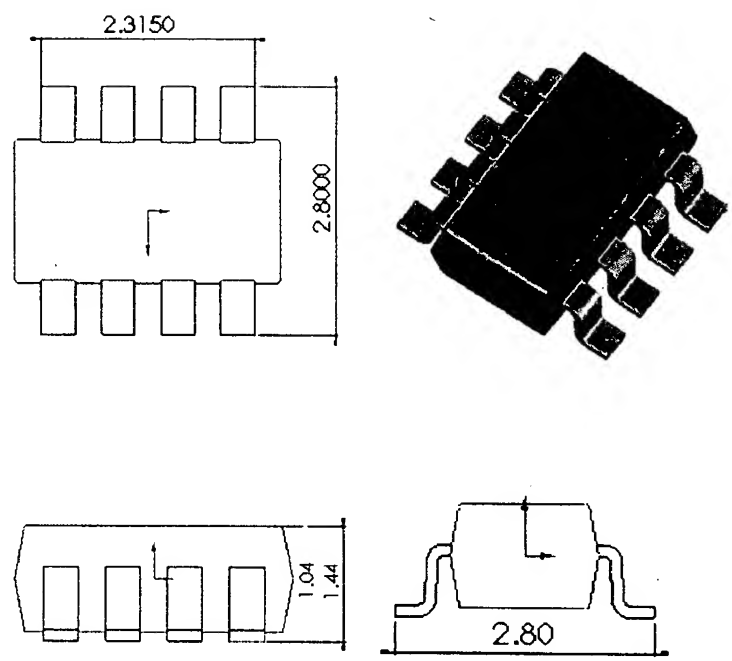


Figure 4a

Comparable TSOP8JW Package

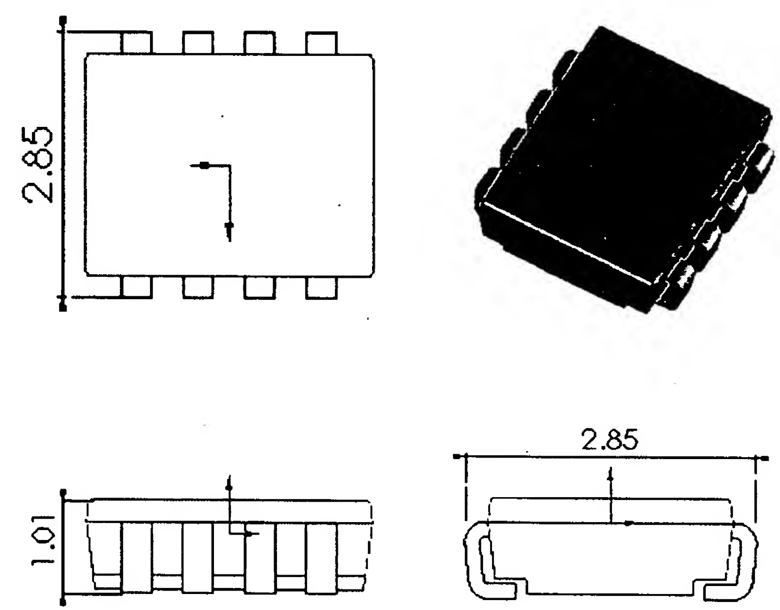


Figure 4b

Internal Structure of GWS6968BW.

FIGURE 5

Figure 5a

cutaway view

Figure 5c

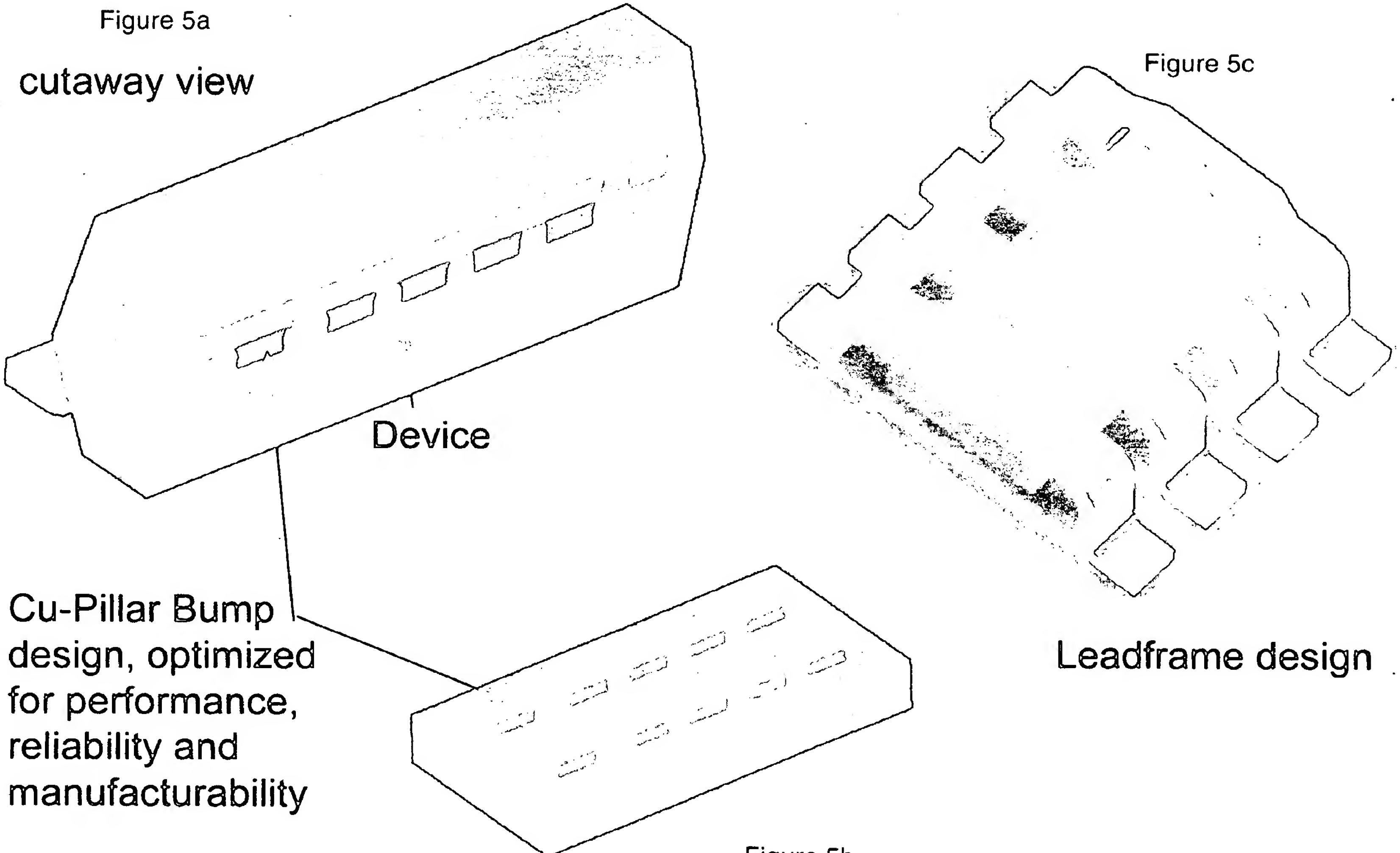


Figure 5b

Symmetry Planes and Key Parameters

FIGURE 6

Refer to Product Specs for detailed dimensions and information.

Figure 6a

GWS6968BW Package

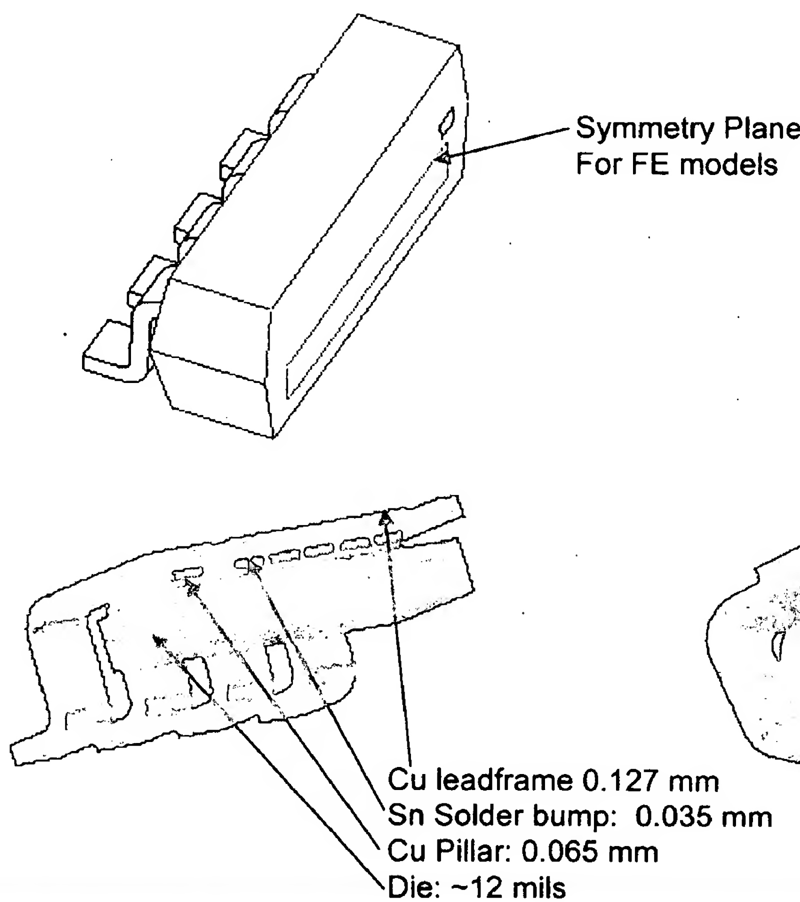
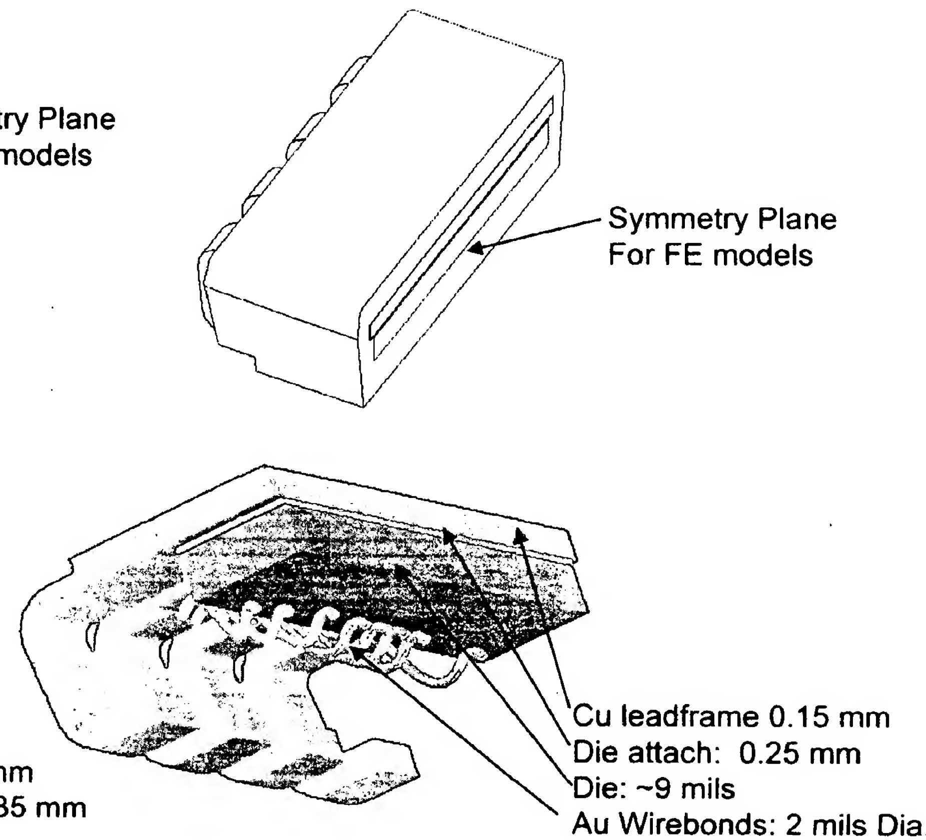


Figure 6b

Comparable TSOP8JW Package

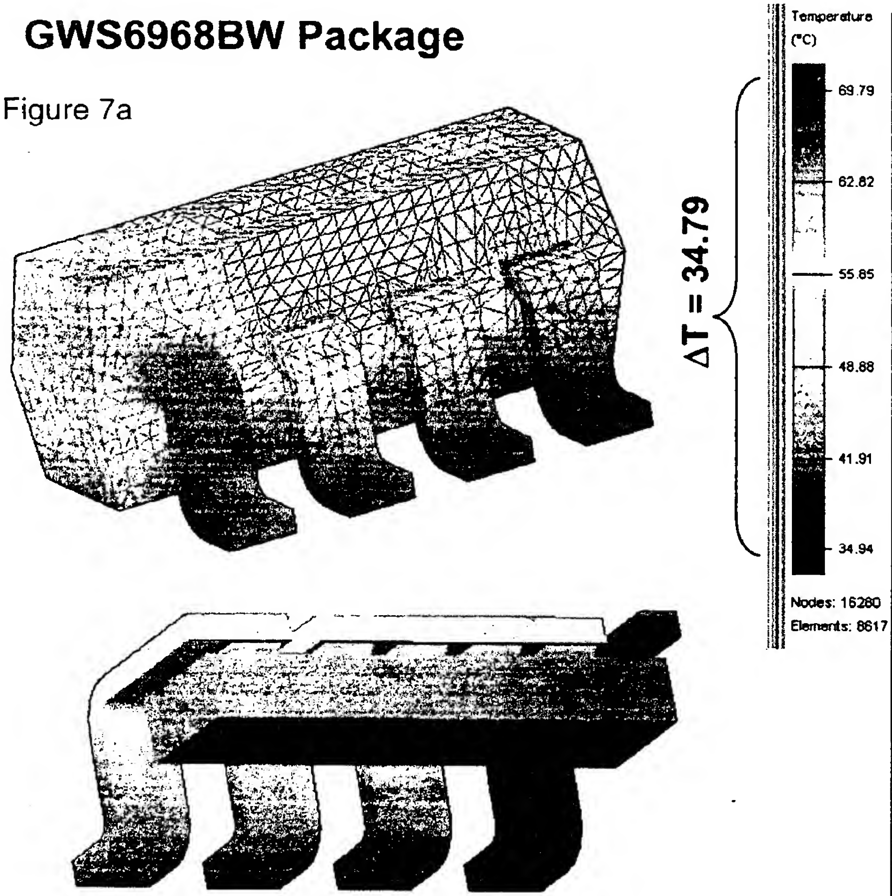


Results: Thermal Resistance

FIGURE 7

GWS6968BW Package

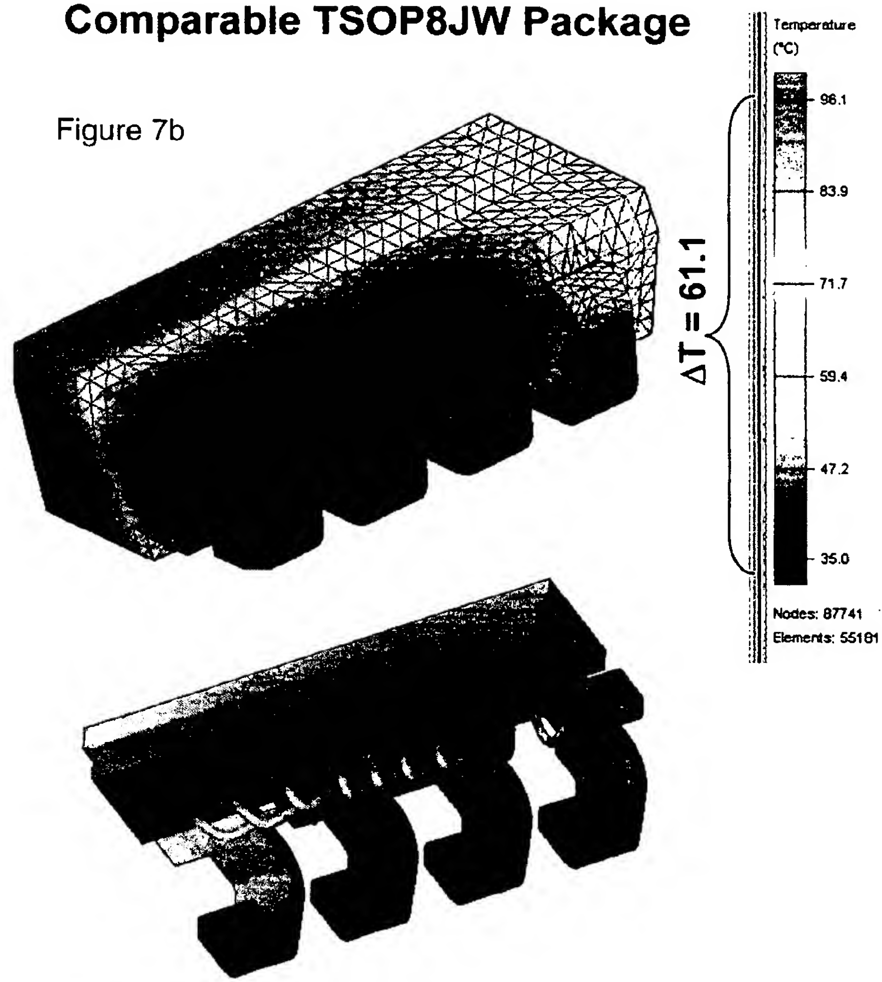
Figure 7a



$$\theta = \frac{\Delta T}{\text{Power}} = 34.79\ ^{\circ}\text{C/W}$$

Comparable TSOP8JW Package

Figure 7b



$$\theta = \frac{\Delta T}{\text{Power}} = 61.1\ ^{\circ}\text{C/W}$$

Summary of Results

FIGURE 8

GWS6869BW Package FEA Results Summary		
Analysis	**TSOP8JW**	**GWS6869BW**
[redacted]		
Electrical Resistance	1.38 mΩ	0.34 mΩ
Stress (self heating)	Pa	Pa
Mold Compound	2.35E+08	7.16E+07
Leadframe	1.06E+08	8.14E+07
Die	2.35E+08	5.73E+07
Solder on Pillars		6.21E+07
Cu Pillars		9.90E+07
Gold wirebonds	2.35E+08	
Die attach	6.51E+07	
Max Displacement	3.1 uM	1.93 uM
Stress (-40C to 25C)		
Mold Compound	2.48E+08	1.28E+08
Leadframe	2.99E+08	3.28E+08
Die	2.48E+08	1.08E+08
Solder on Pillars		1.14E+08
Cu Pillars		1.78E+08
Gold wirebonds	2.48E+08	
Die attach	9.32E+07	
Max Displacement	4.0 uM	5.3 uM
Stress (25C to 85C)		
Mold Compound	2.29E+08	1.18E+08
Leadframe	2.76E+08	3.02E+08
Die	2.29E+08	9.99E+07
Solder on Pillars		1.06E+08
Cu Pillars		1.63E+08
Gold wirebonds	2.29E+08	
Die attach	8.60E+07	
Max Displacement	3.7 uM	4.9 uM

Discussion of Results

FIGURE 9

From several standpoints, the GWS6869BW packaged proposed by Great Wall Semiconductor is superior to a comparable TSOP8JW package, which uses wirebond technology. It is better thermally, electrically and mechanically.

The GWS6869BW has 45% less thermal resistance and 75% less electrical resistance from foot to junction. With respect to stresses, the self induced stress condition is better, between 25% and 75% less, with the GWS6869BW package because operating temperatures are lower. However, stresses induced due to external temperature conditions are comparable between the two packages.

The GWS6869BW design uses a flip-chip die bonding approach on a conventional leadframe. Proven copper pillar bumps technology is employed, allowing for a robust attachment and a simplified manufacturing process. In contrast, the TSOP8JW product requires up to 12 wirebond attachments per product. Wirebonds have historically been a yield and reliability concern due to the low fatigue strength of aluminum and high stress concentrations at the bond heal. The GWS6869BW has no such problems.

Since the Finite Element Analyses Stress performed herein use linear material properties and models, the absolute stress values cannot be taken at face value. Rather a comparison between the two package types is what can be deduced. In actuality, the stresses will be considerably lower due to plasticity of the mold compound. A more detailed model can be generated to account for these phenomenon, but it not recommended at this point. The thermal and electrical modes are fairly accurate since the governing equations are linear with very small second order effects.

One recommendation that can be made is to consider using a higher strength solder on top of the Cu pillars. The current solder, 100% Tin, has a low yield strength, and therefore is susceptible to crack initiation and propagation. A higher strength solder would alleviate this potential problem